Modeling of the Transverse Delays in GaAs MESFET's

ASHOK K. GOEL, MEMBER, IEEE, AND CHARLES R. WESTGATE, SENIOR MEMBER, IEEE

Abstract—**When a signal is applied to the gate electrode in a MESFET, the depletion layer under the gate is not formed instantaneously, resulting in additional propagation delays. We have developed a comprehensive model of these delays in the GaAs MESFET's. The MESFET has been modeled as two lossy transmission lines coupled to each other via the gate–drain capacitances. In addition to the intrinsic MESFET elements, e.g. the internal capacitances and the internal resistances, the model also includes the gate and drain metallization resistances, source and drain contact resistances, and the electrode parasitic capacitances in the MESFET. The electrode capacitances were determined by using the method of moments in conjunction with a Green's function appropriate for the geometry of the MESFET. The model has been used to study the dependence of the delay time and the rise time on the gate length, device width, and resistivity of the gate material. Results can be used for the optimization of high-speed circuits, in particular, picosecond circuits.**

I. Introduction

THE TOTAL propagation delay in a MESFET consists of two parts. First, the time taken by the electrons to move from the source to the drain electrode, usually called the "longitudinal" delay, can easily be calculated by dividing the channel length by the average velocity of the electrons in the channel. This is typically of the order of 3–5 ps. The second part, usually called the "transverse" delay, arises because, at high frequencies, the signal applied to one end of the gate takes a finite time in traveling along the width of the gate. In other words, the depletion layer along the entire width under the gate electrode is not formed instantaneously. Studies [1]–[4] have shown that at frequencies above 10 GHz, one must include the effects of wave propagation along the gate width. A recent study by LaRue *et al.* [4] has shown very clearly that at frequencies above 18 GHz, standing waves exist along the gate width in a GaAs MESFET. That means that, at frequencies above 10 GHz, a lumped-element equivalent circuit for a MESFET will not be adequate to explain the MESFET performance completely and the MESFET should be modeled as a distributed-element equivalent circuit. In the past, equivalent circuits for the GaAs MESFET's valid for microwave frequencies but including only the intrinsic elements in the MESFET have been developed [5]–[7], the MESFET performance including their noise behavior has been studied [8]–[10], and a technique for predicting the large-signal performance of a GaAs MESFET has been presented [11].

In this paper, a model for calculating the transverse propagation delays in GaAs MESFET's, suitable for inclusion in the CAD tools, is developed. The model is suitable for MESFET's with submicron gate lengths as well. First, a distributed-element equivalent circuit for a GaAs MESFET is presented. Then a technique to obtain the transverse delays in the MESFET is developed. The model is then used to find the dependences of the delay and the rise times on the MESFET dimensions and other parameters.

Manuscript received April 17, 1987; revised September 21, 1987, and March 31, 1988. Some of the results given in this paper were presented at the 15 IASTED International Conference on Applied Simulation and Modelling, Santa Barbara, CA, May 27–29, 1987. This work was supported by a research grant from the Westinghouse Electric Corporation.

A. K. Goel is with the Department of Electrical Engineering, Michigan Technological University, Houghton, MI 49931.

C. R. Westgate is with the Department of Electrical and Computer Engineering, The Johns Hopkins University, Baltimore, MD 21218.

IEEE Log Number 8823093.

II. The Model

A. A Distributed-Element Equivalent Circuit for a GaAs MESFET

A GaAs MESFET modeled as two lossy transmission lines coupled to each other by the gate–drain distributed capacitances is shown in Fig. 1. The gate line is fed by an input signal in the form of a unit step voltage on one end while its other end is open circuited. All the elements shown in Fig. 1 are per unit length along the width of the device (denoted by the coordinate z). The circuit includes the intrinsic as well as the extrinsic elements in the MESFET. The various symbols used in Fig. 1 are defined as follows:

R_g	Gate metallization resistance.
R_d	Drain metallization resistance.
L_g	Inductance of the gate line.
L_d	Inductance of the drain line.
C_{gs}	Intrinsic capacitance between the gate and the source electrodes due to the presence of the depletion layer under the gate.
C_{gd}	Intrinsic capacitance between the gate and the drain electrodes.
C_{dc}	Capacitance due to the presence of the dipole layer in the channel of the MESFET.
R_{sc}	Contact resistance of the source electrode.
R_{dc}	Contact resistance of the drain electrode.
r_{gs}	Channel resistance between the gate and source electrodes.
r_{ds}	Channel resistance between the source and drain electrodes.

0018-9480/88/1000-1411$01.00

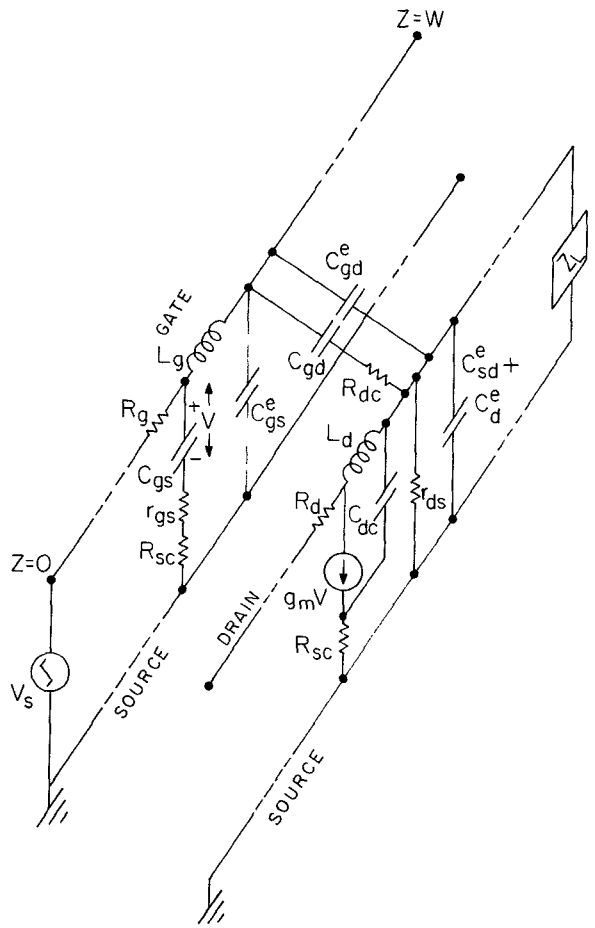


Fig. 1. A GaAs MESFET modeled as two lossy transmission lines coupled to each other by the distributed capacitances C_{gd} and C^e_{gd}. All the elements shown in the figure are per unit length along the width of the device (denoted by the coordinate z).

g_m	Transconductance of the MESFET.
C^e_{gs}	Electrode parasitic capacitance between the source and gate electrodes.
C^e_{gd}	Electrode parasitic capacitance between the gate and drain electrodes.
C^e_{sd}	Electrode parasitic capacitance between the source and drain electrodes.
C^e_d	Self-capacitance of the drain electrode.
V	Voltage across the capacitance C_{gs}.
V_s	A unit step voltage source.
Z_L	Load applied to the drain line.

B. Determination of the Transverse Propagation Delays

In this section, a method for the determination of the transverse propagation delays in a GaAs MESFET is presented. An input signal in the form of a unit step voltage is applied to the gate line as shown in Fig. 1. This signal propagates along the gate line, suffering distortion in its waveform. Due to the presence of the coupling capacitances (C_{gd} and C^e_{gd}) and the transconductance g_m, a distributed current wave is induced in the drain line. Since in a typical MESFET, the gate metal resistance is much higher than that of the drain metal resistance, the induced wave in the drain line propagates at a much higher speed than does the signal in the gate line. In other words, as far as the determination of the propagation delays in the MESFET is concerned, the propagation of the input signal in the gate line decides the speed at which the current at the load end of the drain line reaches its steady-state value. Therefore, in the following analysis, the small resistance and inductance associated with the drain line (L_d and R_d) will be neglected.

In the complex frequency space (the s space), the voltage and current distributions along the gate line satisfy the following transmission line equations:

$$\frac{d^2V_g}{dz^2} = \gamma^2 V_g \tag{1}$$

$$\frac{d^2I_g}{dz^2} = \gamma^2 I_g \tag{2}$$

where γ stands for the propagation constant. Most general solutions of the above differential equations are given by

$$V_g(z) = A\cosh(\gamma z) + B\sinh(\gamma z) \tag{3}$$

and

$$I_g(z) = \frac{1}{Z_0}[A\sinh(\gamma z) - B\cosh(\gamma z)] \tag{4}$$

where Z_0 is the characteristic impedance of the line and the constants A and B can be determined by using the known boundary conditions. In the s space, a unit step is represented by $(1/s)$. Therefore, using the boundary condition at $z = 0$, i.e.,

$$V_g(0) = \frac{1}{s}$$

we get from (3)

$$A = \frac{1}{s}$$

and using the boundary condition at $z = W$,

$$I_g(W) = 0$$

because this end is open circuited, we get from (4)

$$B = \frac{\sinh(\gamma W)}{s\cosh(\gamma W)}.$$

Substituting for A and B in (3) and after simplifying, we get for the voltage along the gate line

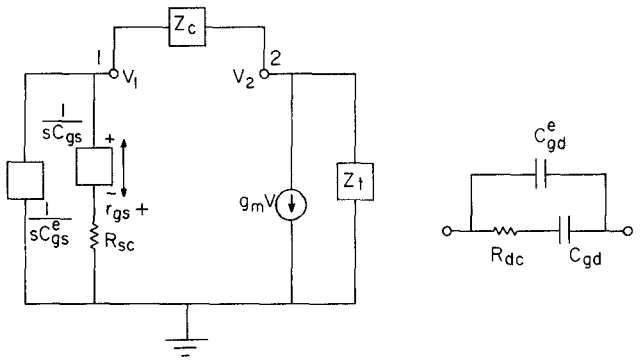
$$V_g(z) = \frac{\cosh\gamma(W - z)}{s\cosh(\gamma W)} \tag{5}$$

C. The Propagation Constant, γ

The propagation constant for a transmission line is given by the equation

$$\gamma = \left\{\frac{Z_s}{Z_p}\right\}^{1/2} \tag{6}$$

where Z_s is the series impedance per unit length along the



(a) (b)

Fig. 2. (a) A section of the gate and drain lines coupled by the impedance Z_c. (b) An equivalent circuit used to obtain the coupling impedance Z_c.

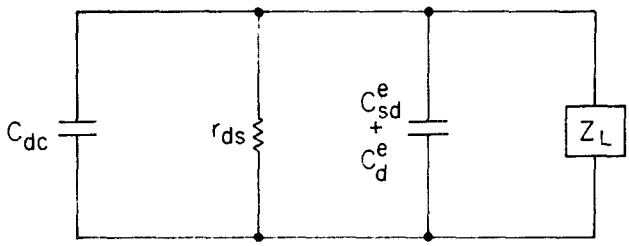


Fig. 3. An equivalent circuit used to obtain the impedance Z_t.

line and Z_p is the parallel impedance per unit length along the line. However, in order to use (6), the line should not be coupled with any other line.

Therefore, the first requirement is to uncouple the gate line from the drain line. This can be accomplished by using Miller's theorem [12]. A section of the gate and drain lines coupled by the impedance Z_c is shown in Fig. 2(a). An equivalent circuit used to obtain Z_c is shown in Fig. 2(b). The ratio between the voltages at nodes 2 and 1, i.e., V_2/V_1, can be found by equating the total current leaving node 2 to zero. This yields

$$\frac{V_2 - V_1}{Z_c} + \frac{V_2}{Z_t} + g_m V = 0 \tag{7}$$

where V is the voltage across the capacitance C_{gs}, and an equivalent circuit used to obtain the impedance Z_t is shown in the Fig. 3. The voltages V_1 and V are related by the expression

$$V = \frac{V_1/sC_{gs}}{r_{gs} + R_{sc} + \dfrac{1}{sC_{gs}}} = kV_1 \quad \text{(say)}. \tag{8}$$

Then (7) becomes

$$V_2\left\{\frac{1}{Z_c} + \frac{1}{Z_t}\right\} = \frac{V_1}{Z_c} - kg_m V_1$$

or

$$K = \frac{V_2}{V_1} = \frac{(1 - kg_m Z_c) Z_t}{Z_t + Z_c}. \tag{9}$$

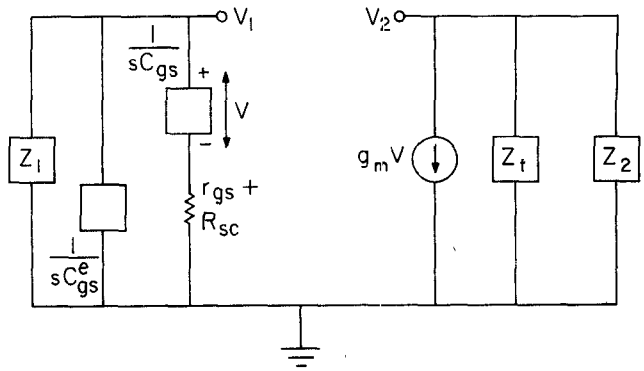


Fig. 4. The uncoupled circuit equivalent to the coupled circuit of Fig. 2(a).

Now, according to Miller's theorem, the circuit of Fig. 2(a) is equivalent to the uncoupled circuit of Fig. 4 provided the impedances Z_1 and Z_2 are given by the following equations:

$$Z_1 = \frac{Z_c}{1 - K}$$

and

$$Z_2 = \frac{Z_c}{1 - \dfrac{1}{K}}.$$

Substituting for K from (9), we get

$$Z_1 = \frac{Z_t - Z_c}{1 - kg_m W Z_t} \tag{10}$$

and

$$Z_2 = \frac{Z_c(1 - kg_m W Z_c) Z_t}{(1 - kg_m W Z_c) Z_t - (Z_t + Z_c)} \tag{11}$$

where W is the width of the MESFET. It has been inserted because g_m has been defined as the transconductance of the MESFET per unit length of the gate line. The series impedance per unit length of the gate line is now given by

$$Z_s = R_g + sL_g \tag{12}$$

whereas the parallel impedance per unit length of the gate line, i.e., Z_p, is equal to the impedance of the parallel combination of Z_1, C_{gs}^e, and the series combination of C_{gs}, r_{gs}, and R_{sc} (see Fig. 4). The propagation constant γ can then be obtained by using (6).

D. Propagation Delays

An indication of the intrinsic speed of the MESFET is given by its short-circuited output current. Current induced in one section of the drain line is given by $-g_m V$, where V, the voltage across the capacitance C_{gs}, is given by (8). Voltage at any point on the gate line, V_g, is given by (5). Therefore, the current induced in one section becomes

$$dI(s) = \frac{-g_m \cosh\gamma(W - z)\, dz}{s\left(1 + sC_{gs}(r_{gs} + R_{sc})\right)\cosh\gamma W}$$

where dz is the length of the section. The total current induced in the drain line will then be given by

$$I(s) = \frac{-g_m}{s\left(1+sC_{gs}\left(r_{gs}+R_{sc}\right)\right)\cosh\left(\gamma W\right)} \cdot \int_0^W \cosh\gamma(W-z)\,dz.$$

After the integration is performed, the expression for $I(s)$ becomes

$$I(s) = \frac{-g_m \tanh\gamma W}{\gamma s\left(1+sC_{gs}\left(r_{gs}+R_{sc}\right)\right)}. \tag{13}$$

The time-domain response of the output current can be obtained by an inverse Laplace transformation of $I(s)$. Because of the presence of branch points associated with the propagation constant γ, inverse transformation will be obtained by using the concept of Bromwich integrals, i.e.,

$$i(t) = \frac{1}{2\pi j}\int_{Br} I(s)\,e^{st}\,ds.$$

Using Simpson's rule, we can write

$$i(t) \approx \frac{1}{2\pi j}\sum_{n=-N}^{+N} I(s)\,e^{st}\Delta s.$$

Writing the complex frequency s in terms of its real and imaginary parts as

$$s = \sigma + j\omega$$

we have

$$\Delta s = j\Delta\omega$$

and

$$s = \sigma + jn\Delta\omega.$$

Therefore

$$i(t) \approx \frac{1}{2\pi}\sum_{n=-N}^{+N} I(\sigma + jn\Delta\omega)\,e^{(\sigma+jn\Delta\omega)t}\Delta\omega. \tag{14}$$

In principle, any positive σ and Δw that will cause two consecutive terms in the summation in (14) to be sufficiently close to each other can be used. However, these were carefully chosen to optimize the speed of convergence. The choice for N depends on the speed of convergence as well but it should be chosen to be sufficiently large.

III. Results and Discussion

A. The Program IPDGM

A program called Intrinsic Propagation Delays in a GaAs MESFET (IPDGM) was written which incorporates the steps of the above section. For given values for the gate length, MESFET width, and electrode material resistivity, the program calculated the propagation constant, performed the summation in (14), and determined the normalized drain current as a function of time in any desired time range. The output response was normalized in the sense that it is the ratio of the output current at a given time t to its value at time $t=\infty$. The program used the following values for the equivalent circuit element:

$$C_{gs} = 1.5\times10^{-9}\ \text{F/m}$$

$$C_{gd} = 4.5\times10^{-11}\ \text{F/m}$$

$$L_g = 10^{-6}\ \text{H/m}$$

$$R_g = 2.0\times\rho\times10^4\ \Omega/\text{m}$$

$$r_{gs} = 3.3\times10^{-3}\ \Omega\cdot\text{m}$$

$$r_{ds} = 0.2\ \Omega\cdot\text{m}$$

$$R_{sc} = 10^{-3}\ \Omega\cdot\text{m}$$

$$R_{dc} = 10^{-3}\ \Omega\cdot\text{m}$$

$$g_m = 100\ \text{S/m}$$

$$C_{dc} = 4.0\times10^{-11}\ \text{F/m}$$

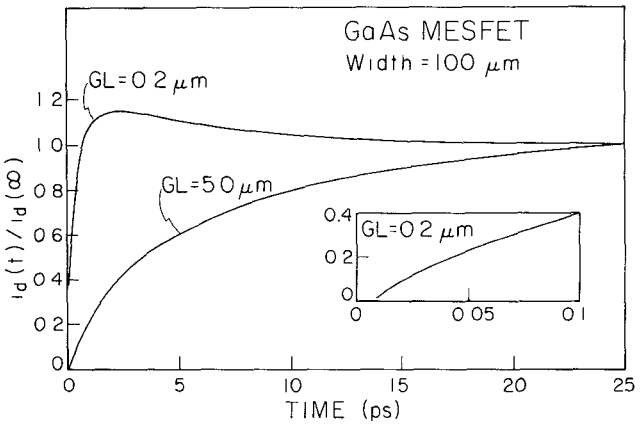


Fig. 5. Normalized short-circuited drain currents in a typical GaAs MESFET for the gate lengths of 0.2 and 5.0 μm. The insert shows the drain current for gate length of 0.2 μm for times less than 0.1 ps.

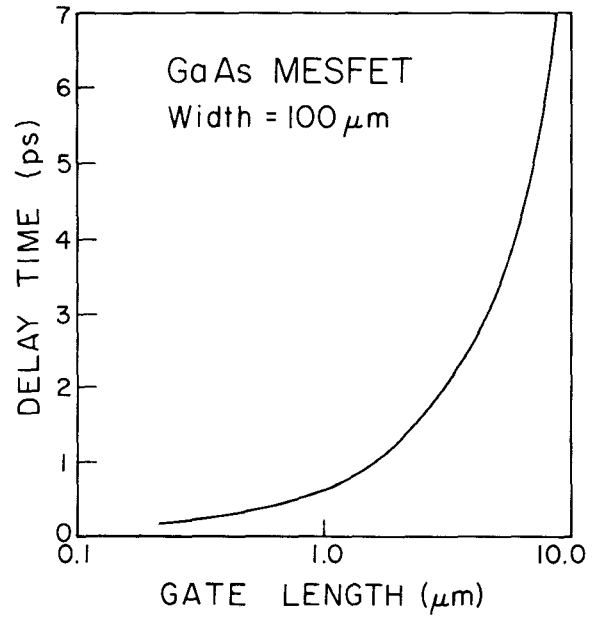


Fig. 6. Dependence of the delay time on the gate length in a typical GaAs MESFET.

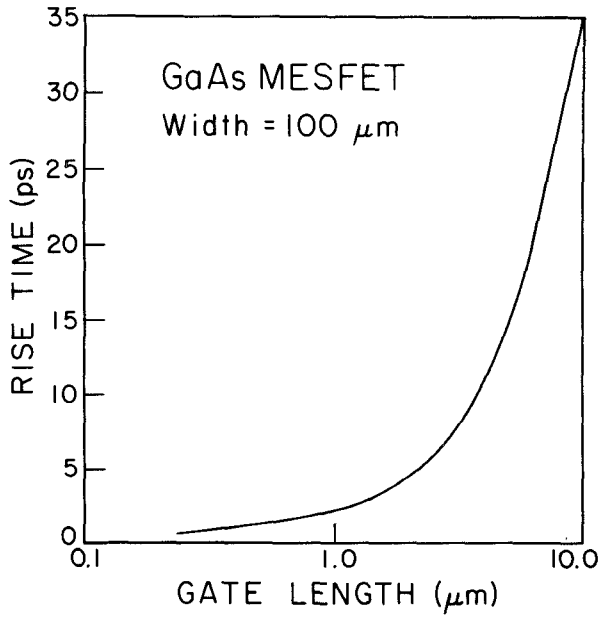


Fig. 7. Dependence of the rise time on the gate length in a typical GaAs MESFET.

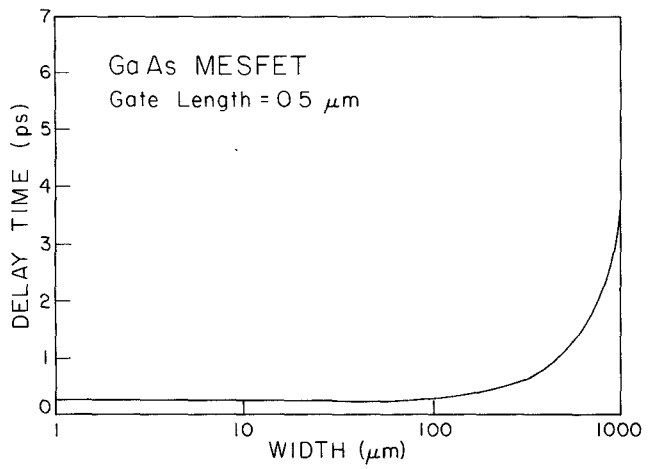


Fig. 8. Delay time in a typical GaAs MESFET as a function of the width of the MESFET.

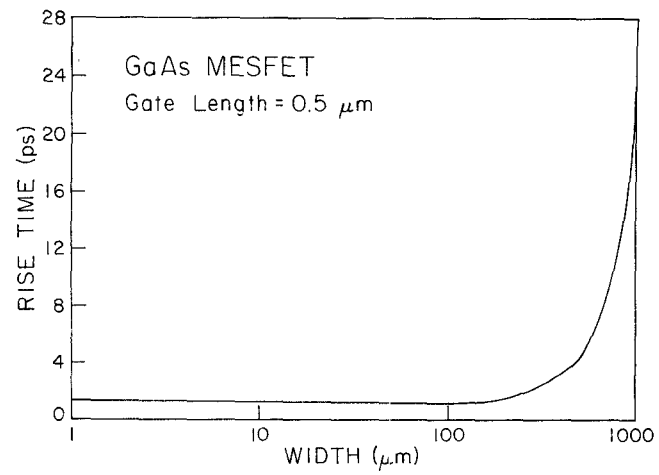


Fig. 9. Rise time in a typical GaAs MESFET as a function of the width of the MESFET.

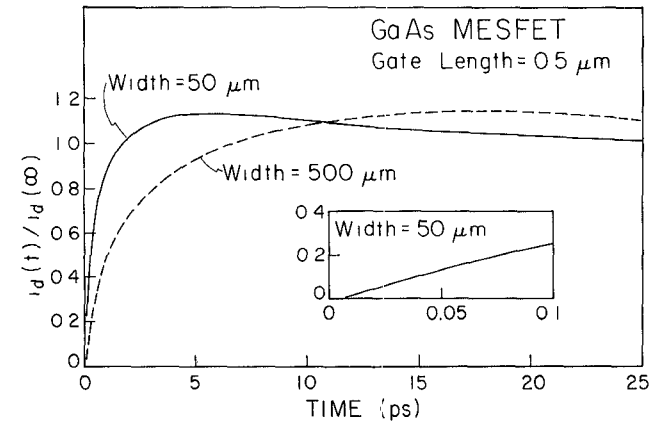


Fig. 10. Normalized short-circuited drain currents in a typical GaAs MESFET for gate widths of 50 and 500 μm. The insert shows the drain current for gate width of 50 μm for times less than 0.1 ps.

where ρ is the electrode material resistivity. All values are per unit length (per meter) of the width of the MESFET. These values represent a typical GaAs MESFET with a 1 μm gate length, 0.5 μm thick gate metal, and $10^{23}/m^3$ channel doping density. The program took care of the fact that the values of C_{gs}, C_{gd}, L_g, and R_g depended on the value of the gate length currently being used. The values of the electrode parasitic capacitances were determined by using the subroutine called EPCSSGM, which was, in fact, the program EPCSGM developed earlier [13].

To optimize the speed of convergence in the summation in (14), it was found that the best values for σ and Δw depended on the time t (in seconds). These were found to be $\sigma = 0.5t$ and $\Delta w = 0.05/t$. The best choice for N depended on t also. It ranged from 200 to 1000 for small t and large t, respectively.

B. Dependence of the Propagation Delays on the MESFET Dimensions and the Electrode Material Resistivity

The program IPDGM has been used to study the dependences of the delay time and the rise time [14] on the MESFET dimensions, namely the gate length and the device width, and on the resistivity of the gate metal. The overshoot and ringing observed in the curves below are due to a finite number of terms included in the approximation expressed by (14) used to find $i(t)$.

Fig. 5 shows the normalized short-circuited output currents for gate lengths of 0.2 and 5 μm. For these results, the width of the MESFET was fixed at 100 μm and the gate metal was taken to be aluminum with $\rho = 3$ μΩ·cm. Fig. 6 shows the dependence of the delay time on the gate length while the dependence of the rise time on the gate length is shown in the Fig. 7. These two figures show that, for gate lengths above 0.5 μm, the delay time and the rise time increase significantly. This increase in the propagation delays can be explained as due to the increase in the capacitances C_{gs} and C_{gd} when the gate length is increased.

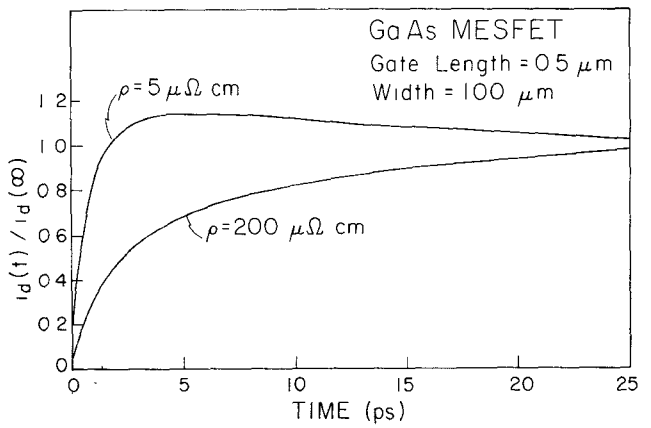


Fig. 11. Normalized short-circuited drain currents in a typical GaAs MESFET for gate metal resistivities of 5 and 200 $\mu\Omega \cdot$cm.

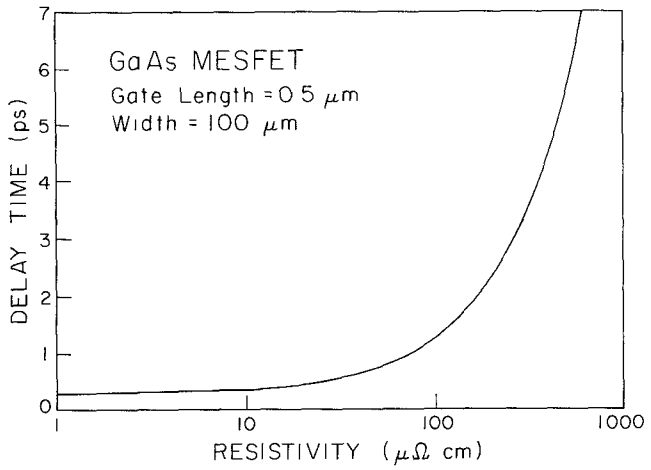


Fig. 12. Delay time in a typical GaAs MESFET as a function of the gate metal resistivity.

As a function of the width of the MESFET, the delay time and the rise time are shown in the Figs. 8 and 9, respectively. Fig. 10 shows the normalized short-circuited output currents for gate widths of 50 and 500 μm. For these results the gate metal was again aluminum and the gate length was fixed at 0.5 μm. Figs. 8 and 9 indicate that the propagation delays increase significantly for device widths greater than 100 μm. This is due to the increase in the capacitances C_{gs} and C_{gd} as the width is increased. For widths less than 100 μm, the propagation times are almost constant as the width is increased.

Fig. 11 shows the normalized short-circuited drain currents for gate metal resistivities of 5 and 200 $\mu\Omega \cdot$cm. For these results, the gate length was fixed at 0.5 μm whereas the width of the MESFET was kept at 100 μm. It shows that, as the resistivity is increased, the drain current rises more slowly toward its steady-state value. The dependences of the delay time and the rise time on the gate metal resistivity are shown in Figs. 12 and 13, respectively.

IV. Summary and Conclusions

A computer-efficient algorithm for calculating the transverse propagation delays in GaAs MESFET's is presented. The MESFET has been modeled as two lossy transmission lines coupled to each other by the gate–drain capacitances. The model is valid for MESFET's with submicron gate lengths as well and is suitable for inclusion in the CAD tools. The algorithm has been used to study the dependences of the transverse propagation delays in GaAs MESFET's on the MESFET dimension and other gate parameters. The results can be utilized for the optimization of high-speed circuits.

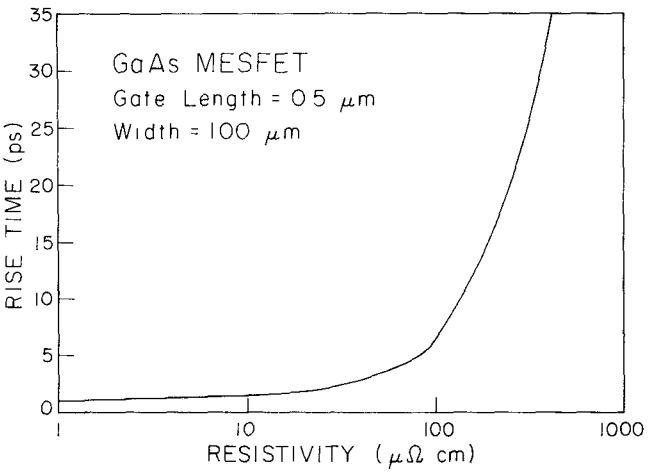


Fig. 13. Rise time in a typical GaAs MESFET as a function of the gate metal resistivity.

Acknowledgment

Many useful comments made by Prof. R. I. Joseph are respectfully acknowledged.

References

[1] P. H. Ladbrooke, "Some effects of wave propagation in the gate of a microwave MESFET," *Electron. Lett.*, vol. 14, pp. 21–22, Jan. 1978.

[2] Y. A. Ren and H. L. Hartnagel, "Wave propagation studies on MESFET electrodes," *Int. J. Electron.*, vol. 51, pp. 663–668, Nov. 1981.

[3] R. L. Kuvas, "Equivalent circuit model of FET including distributed gate effects," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1193–1195, June 1980.

[4] R. LaRue, C. Yuen, and G. Zdasiuk, "Distributed GaAs FET circuit model for broadband and millimeter wave applications," in *1984 IEEE MTT-S Dig.*, pp. 164–166.

[5] R. Dawson, "Equivalent circuit of the Schottky-barrier field-effect transistor at microwave frequencies," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 499–501, June 1975.

[6] G. Vendelin and M. Omori, "Circuit model for the GaAs MESFET valid to 12 GHz," *Electron. Lett.*, vol. 11, pp. 60–61, Feb. 1975.

[7] G. D. Vendelin, "Feedback effects in the GaAs MESFET model," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 383–385, June 1976.

[8] W. Baechtold, "Noise behavior of Schottky barrier gate field-effect transistors at microwave frequencies," *IEEE Trans. Electron Devices*, vol. ED-18, pp. 97–104, Feb. 1971.

[9] W. Baechtold, "Noise behavior of GaAs field-effect with short gate lengths," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 674–680, May 1972.

[10] H. Huang *et al.*, "GaAs MESFET performance," in *1975 Int. Electron Device Meeting, Tech. Dig.*, pp. 235–237.

[11] H A. Willing, C. Rauscher and P. D. Santis, "A technique for predicting large-signal performance of a GaAs FET," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 1017–1023, Dec. 1978.

[12] J. Millman, *Microelectronics*. New York: McGraw-Hill, 1960.

[13] A. K. Goel and C. R. Westgate, "Electrode parasitic capacitances in single-gate GaAs MESFET's," in *Proc Int. Symp. Microelectron.*, 1985, pp. 287–292.

[14] H. E. Kallman and R. E. Spencer, "Transient Response," *Proc. IRE.*, vol. 33, pp. 169–195, 1945.

Ashok K. Goel (S'83–M'86), was born in Punjab, India, on September 4, 1953. He received the B.Sc and M.Sc degrees in physics from the Panjab University, in, respectively, 1972 and 1973, the M. Phil. degree in physics from the City University of New York in 1982, and the Ph.D. degree in electrical engineering from The Johns Hopkins University in 87.

Since 1986, he has been an Assistant Professor in Electrical Engineering at the Michigan Technological University. His current research interests include GaAs-based VLSI, computer-aided design, and solid-state devices, including device physics and modeling.

Charles R. Westgate (M'67-SM'74), was born in Johnson City, NY, in 1940. He received the B.E.E. degree from Rensselaer Polytechnic Institute in 1962 and the Ph.D. degree in electrical engineering from Princeton University in 1966.

Since 1966, he has been a faculty member in the Electrical Engineering Department of The Johns Hopkins University, where he is now Professor and Chair of the Department. His principal research interests include electron devices and circuits, VLSI, and high-speed/microwave circuits.

Dr. Westgate is a member of Tau Beta Pi and Eta Kappa Nu and was named Engineer of the Year (1987) by the Maryland Society of Professional Engineers.